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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,244	12/23/1999	MAGED E. BESHAI	88-882836US	7184
7590	06/15/2005		EXAMINER	
William B Vess Ridout & Maybee One Queen Street East Suite 2400 Toronto, ON M5C3B1 CANADA			HWANG, JOON H	
			ART UNIT	PAPER NUMBER
			2162	
			DATE MAILED: 06/15/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	09/471,244	BESHAI, MAGED E.
	<b>Examiner</b>	<b>Art Unit</b>
	Joon H. Hwang	2162

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 12 July 2004.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 13-24 and 26-43 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 13,14,23,24,28,31,32,34,35 and 37-41 is/are rejected.
- 7) Claim(s) 15-22,26,27,29,30,33,36,42 and 43 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_
- 4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_
- 5) Notice of Informal Patent Application (PTO-152)  
 6) Other: \_\_\_\_\_

### **DETAILED ACTION**

1. The applicant amended claim 18 in the amendment received on 7/12/04.

The pending claims are 13-24 and 26-43.

#### ***Response to Arguments***

2. Applicant's arguments with respect to claims 13-43 have been considered but are moot in view of the new ground(s) of rejection.

#### ***Claim Rejections - 35 USC § 102***

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 13, 32, 34, and 37-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Lampson et al. ("IP Lookups using Multiway and Multicolumn Search", 1998, IEEE, pages 1248-1256).

With respect to claim 13, Lampson teaches a method of resolving B bit long addresses of packets into prefixes of any length up to B by the use of a data structure which comprises a length sorted table Q and a plurality of secondary search units, table Q containing data related to prefixes of length not exceeding A,  $A \leq B$  and each secondary search unit including tables V and T which are in one-to-one correspondence to one another and each comprising a  $2 \times M$  memory, M being a positive integer comprising steps of:

(1) indexing table Q by using the first A bits of an address to generate a corresponding prefix of length equal to or less than A, or a pointer to a secondary search unit (section IV on pages 1251-1252);

(2) accessing table V of the secondary search unit indicated by the pointer using each successive remaining bit of the address in order (i.e., pointers in a node table, section V on pages 1252-1253);

(3) accessing table T of the secondary search unit at each successive location corresponding to the location of table V accessed in step (2) (i.e., key information in a node table, section V on pages 1252-1253); and

(4) reading a valid data contained at the location in table T, the valid data being a prefix of length more than A (section V on pages 1252-1253).

With respect to claim 32, Lampson teaches defining an indexing part comprising a predetermined number of bits (section IV on pages 1251-1252). Lampson teaches indexing a first memory device containing an indexing table based upon the indexing part (section IV on pages 1251-1252). Lampson teaches determining from the indexing translation code, a first pointer, and a second pointer, and if the translation code equals a predetermined value, accessing a secondary memory device from among a plurality of secondary memory devices, the secondary memory device corresponding to the first pointer and storing a plurality of prefixes encoded in at least one tree structure (section I on pages 1248-1249 and section V on pages 1252-1253). Lampson teaches performing a tree-search process on one of the at least one tree structures having a

root defined by the second pointer, wherein the tree-search process identifies the prefix (section V on pages 1252-1253).

With respect to claim 34, Lampson teaches the steps of indexing, determining, and accessing are executed in a sequential temporal order (section V on pages 1252-1253).

With respect to claim 37, Lampson teaches receiving a first address, the address including a first prefix of unknown length and indexing, using a fixed part of the first address, and indexing table Q to read a translation code and data code (section IV on pages 1251-1252). Lampson teaches resolving the data record as a translation if the translation code equals a first predetermined value (section V on pages 1252-1253). Lampson teaches resolving the data record to two identifiers if the translation code equals a second predetermined value, a first of the two identifiers indicating a target secondary search unit in a plurality of secondary search units and the second of the two identifiers indicating a location in the target secondary search unit, and resolving the first address as unknown if the translation code equals a third predetermined value (section V on pages 1252-1253).

With respect to claim 38, Lampson teaches the location in the target secondary search unit corresponds to a root of a branch, the branch comprising prefixes having in common the fixed part of the first address (section V on pages 1252-1253).

With respect to claim 39, Lampson teaches the first address, excluding the fixed part of the first address, is further processed by the target secondary search unit to

resolve the first address to a translation (section IV on pages 1251-1252 and section V on pages 1252-1253).

With respect to claim 40, Lampson teaches receiving a multiplicity of addresses and for each address in the multiplicity of addresses executing the steps of indexing and resolving to two identifiers (section IV on pages 1251-1252).

***Claim Rejections - 35 USC § 103***

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 14, 23-24, 28, 31, 35, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lampson et al. ("IP Lookups using Multiway and Multicolumn Search", 1998, IEEE, pages 1248-1256) in view of Knox et al. ("Parallel Searching Techniques for Routing Table Lookup", 1993, IEEE, pages 1400-1405).

With respect to claim 14, Lampson discloses the claimed subject matter as discussed above except searching in parallel. However, Knox teaches searching for at least two of the addresses in at least two of the secondary search units in parallel (section II on pages 1400-1401 and section III on pages 1401-1403) in order to prevent a delay of matching process from becoming a bottleneck. Therefore, based on Lampson in view of Know, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teaching of Knox to the system of Lampson in order to prevent a delay of matching process from becoming a bottleneck.

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With respect to claim 23, Lampson teaches a parsing block for receiving the packet and parsing an address of the packet, the address having length B, B being a positive integer (section I on pages 1248-1249). Lampson teaches an indexing block for directly accessing a sorted prefix directory by the first A binary bits, A<B, the sorted prefix directory containing translated prefixes of length not exceeding A and data specifying one of a plurality of secondary search units (section IV on pages 1251-1252). Lampson teaches plurality of secondary search units each having a secondary memory for searching for different prefixes of length grater than A (section V on pages 1252-1253), wherein each secondary memory comprises tables V and T containing interleaved tree branches, each of the tree branches corresponding to an entry in the sorted prefix directory (section V on pages 1252-1253). Lampson does not explicitly disclose searching in parallel. However, Knox teaches performing routing table lookup searches in parallel (section II on pages 1400-1401 and section III on pages 1401-1403) in order to prevent a delay of matching process from becoming a bottleneck. Therefore, based on Lampson in view of Know, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teaching of Knox to the system of Lampson in order to prevent a delay of matching process from becoming a bottleneck.

With respect to claim 24, Lampson further teaches each prefix of length longer than A belongs to a specific branch and each secondary memory contains prefixes of at least one branch (section IV on pages 1251-1252).

With respect to claim 28, Lampson teaches an address separation unit for separating from a packet an address to be translated (section I on pages 1248-1249). Lampson teaches primary translation unit having a primary translation table for translating the address to a prefix, the primary translation table containing prefixes whose widths are less than a predetermined value and locations of branch search data structures in a secondary search units (section IV on pages 1251-1252). Lampson teaches a plurality of secondary search units for performing secondary searches, each secondary unit having the branch search data structure for performing each secondary search and translating the address to a prefix, if the primary translation table indicates the location of a branch search data structure to being the secondary search (section V on pages 1252-1253). Lampson does not explicitly disclose searching in parallel. However, Knox teaches performing routing table lookup searches in parallel (section II on pages 1400-1401 and section III on pages 1401-1403) in order to prevent a delay of matching process from becoming a bottleneck. Therefore, based on Lampson in view of Know, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teaching of Knox to the system of Lampson in order to prevent a delay of matching process from becoming a bottleneck.

With respect to claim 31, Lampson further teaches the secondary searches are performed for a number of distinct addresses not exceeding the number of secondary search units in the plurality of secondary search units (section V on pages 1252-1253). The limitations are rejected in the analysis of claim 28 above, and the claim is rejected on that basis.

With respect to claim 35, Lampson teaches the tree-search process for one of the addresses is performed with the tree-search process for at least one other of the addresses in at least two of the secondary memory devices (section V on pages 1252-1253). Lampson does not explicitly disclose searching concurrently. However, Knox teaches performing routing table lookup searches concurrently (section II on pages 1400-1401 and section III on pages 1401-1403) in order to prevent a delay of matching process from becoming a bottleneck. Therefore, based on Lampson in view of Know, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teaching of Knox to the system of Lampson in order to prevent a delay of matching process from becoming a bottleneck.

With respect to claim 41, Lampson teaches at least two of the secondary search units process at least two addresses in the multiplicity of address (section V on pages 1252-1253). Lampson does not explicitly disclose searching concurrently. However, Knox teaches performing routing table lookup searches concurrently (section II on pages 1400-1401 and section III on pages 1401-1403) in order to prevent a delay of matching process from becoming a bottleneck. Therefore, based on Lampson in view of Know, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teaching of Knox to the system of Lampson in order to prevent a delay of matching process from becoming a bottleneck.

***Allowable Subject Matter***

7. Claims 15-22, 26-27, 29-30, 33, 36, and 42-43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joon H. Hwang whose telephone number is 571-272-4036. The examiner can normally be reached on 9:30-6:00(M~F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JOHN E. BREENE can be reached on 571-272-4107. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joon Hwang  
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6/10/05



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PRIMARY EXAMINER